29. Multimedia interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a media processor block incorporated on the IC chip; and

audio and/or video CODEC incorporated on the IC chip for interfacing to external analog signals.

30. Multimedia interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a media processor block incorporated on the IC chip; and

phase locked loop (PLL) circuitry incorporated on the IC chip to reduce skew within various blocks within the IC chip.

31. Multimedia interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a media processor block incorporated on the IC chip; and

a programmable, fast serial interface core incorporated on the IC chip.

32. Multimedia interface according to claim 31, wherein:

the programmable, fast serial interface core is incorporated within the reconfigurable logic block.

33. Multimedia interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a media processor block incorporated on the IC chip; and

a programmable CPU interface core incorporated on the IC chip.

34. Multimedia interface according to claim 33, wherein:

the programmable CPU interface core is incorporated within the reconfigurable logic block.

35. Multimedia interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a media processor block incorporated on the IC chip; and

a programmable memory interface (PMI) core incorporated on the IC chip.

36. Multimedia interface according to claim 35, wherein:

the programmable memory interface core is incorporated within the reconfigurable logic block.

37. Multimedia interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a media processor block incorporated on the IC chip; and

at least one additional core selected from the group consisting of

audio and/or video CODECs for interfacing to external analog signals;

phase locked loop (PLL) circuitry to reduce skew within various blocks within the IC chip;

a programmable, fast serial interface core;

a programmable CPU interface core;

a programmable memory interface (PMI) core; and

further comprising power-down circuitry, in combination with one or more of these additional cores, incorporated on the IC chip to provide power and/or processing savings when a given one of the cores is not in use.

38. Signal processing interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a RISC core incorporated on the IC chip; and

audio and/or video CODEC for interfacing to external analog signals incorporated on the IC chip.

39. Signal processing interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a RISC core incorporated on the IC chip; and

phase locked loop (PLL) circuitry incorporated on the IC chip to reduce skew within various blocks within the IC chip.

40. Signal processing interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a RISC core incorporated on the IC chip; and

a programmable, fast serial interface core incorporated on the IC chip.

41. Signal processing interface according to claim 40, wherein:

the programmable, fast serial interface core is incorporated within the reconfigurable logic block.

42. Signal processing interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a RISC core incorporated on the IC chip; and

a programmable CPU interface core incorporated on the IC chip.

43. Signal processing interface according to claim 42, wherein:

the programmable CPU interface core is incorporated within the reconfigurable logic block.

44. Signal processing interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a RISC core incorporated on the IC chip; and

a programmable memory interface (PMI) core incorporated on the IC chip.

45. Signal processing interface according to claim 44, wherein:

the programmable memory interface core is incorporated within the reconfigurable logic block.

B1

A2

end

46. Signal processing interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a RISC core incorporated on the IC chip; and

at least one additional core selected from the group consisting of

audio and/or video CODEC for interfacing to external analog signals;

phase locked loop (PLL) circuitry to reduce skew within various blocks within the IC chip;

a programmable, fast serial interface core;

a programmable CPU interface core;

a programmable memory interface (PMI) core; and

further comprising power-down circuitry, in combination with one or more of these additional cores, incorporated on the IC chip to provide power and/or processing savings when a given one of the cores is not in use.

IN THE SPECIFICATION

Replace the original title, at page 1, line 0 ("MULTIMEDIA FPGA") with:

-- MULTIMEDIA INTERFACE HAVING A PROCESSOR AND RECONFIGURABLE LOGIC --

(and please delete the docket number at the extreme top left of page 1)